

REMARKS

At the outset, Applicants thank the Examiner for the thorough review and consideration of the subject application. The Final Office Action of April 6, 2004 has been received and its contents carefully reviewed.

In the Final Office Action, the Examiner rejected claims 1, 2, 4, 6, 8, 9, 11, 20, and 21 under 35 U.S.C. § 102(e) as being anticipated by Shin (U.S. Patent No. 6,323,836); rejected claims 3, 5, 7, 10, and 12 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Nakano et al. (U.S. Patent No. 6,229,513); and rejected claims 13-19 under 35 U.S.C. § 103(a) as being unpatentable over Nakano et al. in view of the Related Art shown in Figure 3. The rejections of these claims are traversed and reconsideration of the claims is respectfully requested in view of the following remarks.

The rejection of claims 1, 2, 4, 6, 8, 9, 11, 20, and 21 under 35 U.S.C. § 102(e) as being anticipated by Shin is traversed and reconsideration is respectfully requested.

Independent claim 1 is allowable over Shin in that claim 1 recites a combination of elements including, for example, “a timing controller... for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of said line memory to the driving circuit every period of the data clock...” Shin fails to teach, either expressly or inherently, at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claims 2, 4, and 6, which depend from claim 1, are also allowable over Shin.

Independent claim 8 is allowable over Shin in that claim 8 recites a combination of elements including, for example, “a timing controller... for receiving a data clock inputted from the exterior thereof to generate a first data clock by frequency-dividing the data clock... and for outputting the data in each of the groups to the driving circuit during each period of the input data clock.” Shin fails to teach, either expressly or inherently, at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claims 9 and 11, which depend from claim 8, are also allowable over Shin.

Independent claim 20 is allowable over Shin in that claim 20 recites a combination of elements including, for example, “a data clock generating step of frequency-dividing an input first data clock at a frequency-division ratio... to generated a second data clock; a data outputting step of outputting a desired data unit from each of said groups at a different time during one period of the second data clock...” Shin fails to teach, either expressly or inherently,

at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claim 21, which depends from claim 20, is also allowable over Shin.

In rejecting claims 1, 8, and 20, the Examiner alleges that Shin teaches “a timing controller (220), being connected to the line memory (230) and the driving circuit (270), for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of the line memory (230) to the driving circuit (270) every period of the data clock... (see column 5, line 18-column 6, line 18).”

Further, in the “Response to Arguments” section of the present Office Action, the Examiner attempts to support the rejection of claims 1 and 8 by asserting that “the claim recites that the timing controller receives *a data clock* inputted from the exterior thereof, and the driving circuit outputs data every period of *the data clock*. The claim does not recite *the data clock* as *said data clock*, which would be that which is inputted from the exterior. *The data clock* is the data clock in which the driving circuit outputs data according to. Applicants respectfully disagree with the substance of the Examiner’s aforementioned allegation and submit the following.

Preliminarily, Applicants respectfully submit the difference between the terms “the” and “said,” without more, cannot logically imply the use of different types of data clocks. Applicants respectfully request the Examiner to clarify exactly how the term “*the data clock*” can refer to something different from the term “*said data clock*.”

Referring to claim 1, the term “data clock” within the phrase “to output the data... to the driving circuit every period of the data clock” implicitly refers to the term “data clock” within the phrase “for receiving a data clock inputted from the exterior thereof” as there is no other preceding occurrence of the term. Referring to claim 8, the term “input data clock” within the phrase “for outputting the data... to the driving circuit during each period of the input data clock” implicitly refers to the term “data clock” within the phrase “for receiving a data clock inputted from the exterior thereof.” It should be noted that “first data clock” of claim 8 cannot be reasonably construed as the “input data clock” since the “first data clock” is generated “by frequency-dividing the input data clock.”

As described above, each type of data clock used in each claim has been clearly defined within each claim. Accordingly, Applicants respectfully submit that the scope of the claims is definite regardless of whether “data clock” is preceded by the term “the” or “said.”

Moreover, the “data clock” to which the Examiner refers in stating that Shin teaches “a timing controller (220)... for receiving a data clock inputted from the exterior thereof” corresponds to the “first clock signal CK1,” illustrated in Figures 7 and 8 and described at column 5, lines 28-31 and 54-59 of Shin. The Examiner also acknowledges this at lines 5-7 of paragraph 7 on page 7 of the Non-Final Office Action dated October 22, 2003 (i.e., the Non-Final Office Action).

Referring in detail to Figures 7 and 8 and column 5, line 28 - column 6, line 18 of Shin, the first clock signal CK1 is in input to the controller 220 (see Shin, Figures 7 and 8, column 5, lines 28-31 and 54-59; Non-Final Office Action, lines 5-7 of paragraph 7 on page 7). Accordingly, the first clock signal CK1 is input from the exterior of the controller 220. The controller 220 uses the first clock signal CK1 to generate the second clock signal CK2 (see Shin, Figures 7 and 8 and column 5, lines 31-32, 59-63; Non-Final Office Action, lines 9-10 of paragraph 7 on page 7). Moreover, data is output to a driving circuit every period of the second clock signal CK2 (see Shin, Figure 8 and column 5, line 66 - column 6, line 2; Non-Final Office Action, lines 11-13). Figure 8 of Shin distinctly shows wherein data d1-d4 is output at output terminals D1 and D2 (see Shin, Figure 7, column 5, lines 28-35) every period of the second clock signal CK2 (i.e., every period of a clock signal generated by an externally inputted clock signal), or every other period of the first clock signal CK1 (i.e., every other period of an externally inputted clock signal). Applicants respectfully note that those of ordinary skill in the art recognize the term “period,” within the present context, represents a time interval between two successive occurrences of a recurrent event.

In view of actual recitations of claims 1 and 8, and in view of the actual teachings of Shin, Applicants respectfully submit Shin fails to anticipate each and every element as set forth in the claims.

In the “Response to Arguments” section of the present Office Action, the Examiner states that the related art shown in Figures 2 and 3 teach “data being output to the driving circuit every period of the data clock received externally thereof.” Applicant disagrees.

Referring to the related art shown in Figure 1, ODD DATA, EVEN DATA, and a data clock (DCLK1 of line (a) in related art shown in Figure 2 - see page 3, lines 18-20; page 5, lines 1-5) are input to the timing controller 10 (see page 3, lines 9-10). Accordingly, the aforementioned data clocks are input from the exterior of the timing controller 10. Moreover, a

twice-frequency-divided data clock DCLK2 (see Figure 2, line (c); page 3, lines 18-22) and a two-frequency-divided source sampling clock SSC (see Figure 3, line (d); page 5, lines 1-5) (both generically referred to as frequency divided clocks) are output from the timing controller 10 to the driving circuit 20. Referring to the related art shown in either of Figures 2 or 3, data is output to the driving circuit every period of the frequency divided clock (Figure 2, lines (d) and (e)/ Figure 3, lines (c), (d), (f), and (g)) or every other period of the externally input data clock. Applicants respectfully note that those of ordinary skill in the art recognize the term “period,” within the present context, represents a time interval between two successive occurrences of a recurrent event.

In view of the actual teachings of the related art shown in Figures 2 and 3, Applicants respectfully submit the related art shown in Figures 2 and 3 fails to teach “data being output every period of the data clock received externally thereof,” as asserted by the Examiner.

In the “Response to Arguments” section of the present Office Action, the Examiner attempts to respond to Applicants argument that “claims 1 and 8 do not recite any element suggesting that data is outputted every period of a clock signal generated from an externally inputted clock signal” by asserting that Figure 6 of the present application allegedly shows where “data is output to the driving circuit every period of the data clocks SSC1 and SSC2.”

It is respectfully submitted, however, that the contents of Figure 6 are not in dispute. The actual recitations of claims 1 and 8, in this instance, however, are. Applicants respectfully direct the Examiner’s attention to the above-cited analysis of claims 1 and 8 and respectfully submit that Figure 6 clearly, and in an exemplary manner, illustrates what is actually claimed while the present claims do not recite absolutely everything illustrated in Figure 6. For illustrative purposes only, ODD DATA, EVEN DATA, and a data clock DLCK are input to the timing controller 410 (see Figure 4). Accordingly, the data clock DLCK is input from the exterior of the timing controller 410. Moreover, the first and second sampling clocks SSC1 and SSC2 are output (see Figure 6, lines (b) and (e)) from the timing controller 410 to the driving circuit 20. Referring to Figure 6 of the present application, data is output to the driving circuit every period of the first and second sampling clocks SSC1 and SSC2 (see lines (c), (d), (f), and (g)). However, data is also output every period of the externally input data clock DLCK (see line (a)).

For at least these reasons, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 102.

Further, in rejecting claim 20, the Examiner cites Shin as allegedly teaching “generating a first data clock by frequency-dividing the data clock at a frequency-division ratio corresponding to the number of divided groups (see column 3, lines 53-62). In the “Response to Arguments” section of the present Office Action, the Examiner further states that Shin allegedly teaches “a driving circuit for including a clock generator for processing a first clock signal to output a second clock signal, the clock speed of the second clock signal being on Nth of that of the first clock signal.”

Notwithstanding the alleged teachings of Shin, Shin still fails to teach each and every element as set forth in claim 20. For example, claim 20 recites, among other elements, “a data clock generating step... to generate a second data clock; [and] a data outputting step of outputting a desired data unit from each of said groups at a different time during one period of the second data clock.” Shin does not teach at least these features of claim 20. For example, Figure 8 of Shin teaches wherein data is output from terminals D1 and D2 at the same time during one period of second data clock CK2. It is respectfully submitted that signals which are output at the same time cannot be output at different times during one period of a data clock. Accordingly, in this case, a device outputting signals at the same time during one period of a data clock cannot anticipate a device outputting signals at different times during one period of a data clock.

For at least these reasons, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 102.

The rejection of claims 3, 5, 7, 10, and 12 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Nakano et al. is traversed and reconsideration is respectfully requested.

Applicants respectfully submit that claims 3, 5, 7, 10, and 12 are allowable at least because these claims depend from independent claims 1 and 8, which are believed to be allowable.

The rejection of claims 13-19 under 35 U.S.C. § 103(a) as being unpatentable over Nakano et al. in view of the Related Art shown in Figure 3 is traversed and reconsideration is respectfully requested.

Independent claim 13 is allowable over Nakano et al. in view of the Related Art shown in Figure 3 in that claim 13 recites a combination of elements including, for example, “a timing

controller... connected to the line memory and the driving circuit, for receiving a data clock inputted from the exterior thereof to generate a first data clock by frequency-dividing the input data clock... and for outputting the two pixel data in each of the groups to the driving circuit during each period of the input data clock.” Neither Nakano et al. nor the Related Art shown in Figure 3, singly or in combination, teach or suggest at least these features of the claimed invention. Accordingly, Applicants respectfully submit that claims 14-17, which depend from claim 13 are also allowable over Nakano et al. in view of the Related Art shown in Figure 3.

Independent claim 18 is allowable over Nakano et al. in view of the Related Art shown in Figure 3 in that claim 18 recites a combination of elements including, for example, “a timing controller... connected to the latch circuit and the driving circuit, for receiving a data clock inputted from the exterior thereof to output each one pixel data to the driving circuit at a desired time interval during one period of the data clock.” Neither Nakano et al. nor the Related Art shown in Figure 3, singly or in combination, teach or suggest at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claim 19, which depends from claim 18, is also allowable over Nakano et al. in view of the Related Art shown in Figure 3.

In rejecting claims 13 and 18, the Examiner cites Nakano et al. as allegedly teaching “a first and second memory (112, 113) for receiving and storing originally ordered display data transmitted from the computer side. The data is then outputted to the drain drivers (130) through the display bus line (134) (see column 7, lines 3-17). Drivers (130)... are connected between the liquid crystal panel (10) and (memory (112, 113) comprised in the display control unit (110) (see column 6, lines 16-37). Within the display control unit (110) a clock signal (CK) is transmitted from the computer side, and is divided by a D-type flip flop (11) such that clock signals (D4, D5) are half the frequency of the original clock signal (CK).” The Examiner also cites Nakano et al. as failing to teach “that the memory receives two-pixel data unit, or that the driving circuit includes n driver integrated circuits.” In an apparent attempt to cure this deficiency, the Examiner states Nakano et al. “does... teach that the first and second memories (112, 113) stores display data of an amount corresponding to a total number (2n) of the drain signal lines (D) connected to two drain drivers (130)” and “with reference to a second embodiment, a liquid crystal display of higher resolution has two bus lines (134a, b) as display data bus lines, and drain drivers (130') are connected thereto (see column 7, lines 43-50).”

Regardless of whatever Nakano et al. may teach, Applicants respectfully submit, however, that Nakano et al. also fails to teach or suggest each and every element as actually set forth in claims 13 and 18.

For example, column 7, lines 43-50 of Nakano et al. includes the textual passage apparently corresponding to the alleged “second embodiment” of Nakano et al. describing what is illustrated in Figures 5A and 5B of Nakano et al. At column 3, lines 41-45 in the BRIEF DESCRIPTION OF THE DRAWINGS section, Nakano et al. states “FIG. 5A is a block diagram illustrating an exemplary approach, considered by the present inventors and others, for transmitting a display data from the display control unit to drain drivers...” Accordingly, Applicants respectfully submit the disclosure of Nakano et al. directed to Figures 5A and 5B actually disclose what is admitted to be conventional art. At column 7, line 58 – column 8, line 2, Nakano et al. states

“The approach illustrated in FIGS. 5A, 5B, however, requires a twice wider bus width for the display data bus line..., thereby causing an increase in the number of pins required for the display control unit 110, an increase in the number of layers and the area of the printed wiring board, on which the display control unit 110 is mounted. This further leads to an increase cost for the display control unit 110 and the associated printed wiring board, and a larger size of a connector attached to the printed wiring board...”

Accordingly, Applicants respectfully submit the “second embodiment” cited by the Examiner is equivalent to a “prior art embodiment” which teaches away from the actual inventive concept as taught by Nakano et al. at column 4, line 32 through column 7, line 42. Therefore, Applicants respectfully submit the “second embodiment” of Nakano et al. cannot, absent impermissible hindsight reasoning, be combined with the inventive concept of Nakano et al. to arrive at the combination of elements in the present invention. For at least these reasons, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 103(a).

In the “Response to Arguments” section of the present Office Action, and in response to Applicants preceding argument, the Examiner states “[Nakano et al.] teaches all that is required by the claim except, that the memory receives two-pixel data unit... but teaches with reference to a different embodiment that the first and second memories (112, 113) stores display data of an amount corresponding to a total number (2n) of the drain signal lines (D) connected to two drain drivers (130)” (as will be discussed in greater detail below, Nakano et al. does not teach “all that

is required,” save the noted exceptions, as asserted by the Examiner). In light of the teachings of the Nakano et al. the Examiner concludes, that

“there is a suggestion that it is possible for the memory to receive two pixel data units from the exterior thereof and dividing the data for at least one line into a plurality of groups to store the divided data therein and for outputting the two pixel data unit from each of the groups, since it is possible for the memories to store display data of an amount corresponding to the total number of the drain signal lines, in order to increase the resolution of the driven display...”

Applicants respectfully submit, however, that Nakano et al. teaches, at column 7, lines 3-17 wherein

“...originally ordered display data transmitted from the computer side are inputted to a first memory 112 (or a second memory 113). The first memory 112 (and the second memory 113) stores display data of an amount corresponding to a total number $2n$ of the drain signal lines D connected to two drain drivers 130 (n being a positive integer).

In the example illustrated in FIG. 4A, the $2n$ originally ordered display data transmitted from the computer side are first written, for example, into the first memory 112. When $2n$ display data are stored in the first memory 112, next $2n$ display data transmitted from the computer side are written into the second memory 113, and meanwhile the display data are read from the first memory 112 in an order shown in FIG. 4B and outputted to the drain drivers 130 through the display data bus line 134.”

Accordingly, Applicants respectfully submit Nakano et al. can be reasonably understood as disclosing, with respect to Figures 4A and 4B, a memory that receives a single exterior pixel data unit which is subsequently divided. However, it is respectfully submitted that Nakano et al. cannot be reasonably interpreted as teaching or even suggesting that a timing controller receives two exterior pixel data units, divides the data for at least one line into a plurality of groups, and stores the divided data therein as required, at least in part, by claim 13. Similarly, Applicants respectfully submit Nakano et al. cannot be reasonably interpreted as teaching or even suggesting a timing controller for outputting two externally inputted pixel units as required, at least in part, by claim 18. Stated another way, that Nakano et al. allegedly teaches “first and second memories (112, 113)... [that store] data of an amount corresponding to a total number ($2n$) of... drain signal lines (D) connected to two drain drivers (130)” cannot, without more,

either explicitly or implicitly teach or suggest the existence of either a timing controller that a timing controller receives two exterior pixel data units, divides the data for at least one line into a plurality of groups, and stores the divided data therein as required, at least in part, by claim 13 or the existence of a latch circuit for latching and outputting two externally input pixel unit or a timing controller for outputting the two externally inputted pixel units as required, at least in part, by claim 18.

For at least these reasons, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 103(a).

Further, assuming *arguendo* that Nakano et al. provides a suggestion that it is possible for “memory to receive two pixel data units from the exterior thereof and dividing the data... into a plurality of groups... and for outputting the two pixel data unit from each of the groups,” Applicants respectfully submits Nakano et al. fails to provide a suggestion that the “memory” is capable of “outputting the two pixel data in each of the groups... during each period of the input data clock,” as recited in claim 13 or “[outputting] each one pixel data ... at a desired time interval during one period of the data clock,” as recited in claim 18. Please note that the “data clock” in each of the above-cited passages in claims 13 and 18 explicitly refers to data clocks, the sources of which are exterior to the timing controller. As described above with respect to the related art shown in Figures 2 and 3, data from each of the different groups is not output during each period of an externally input data clock. Stated another way, each one pixel data is not output during one period of the data clock. Similarly, referring to Figure 5B of Nakano et al., data from each of the groups is output every other period of an externally input data clock CK. Because neither Nakano et al. nor the related art shown in Figures 2 and 3 teach or suggest at least these features of the claimed invention, Applicants respectfully submit that their combination does not teach or suggest at least these features of the claimed invention.

For at least these reasons, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 103(a).

Claim 14 depends from independent claim 13 and, therefore, includes at least the aforementioned combination of elements set forth in claim 13. As described above Nakano et al. fails to teach at least the aforementioned combination of claimed elements. The Related Art shown in Figure 3 was cited as allegedly disclosing the various elements of claim 14. Even if the Related Art shown in Figure 3 actually does disclose the various elements asserted by the

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Examiner, the Applicant respectfully submits the Related Art shown in Figure 3 fails to cure the aforementioned deficiencies of Nakano et al. Accordingly, the Applicant respectfully submits that claim 14 is allowable over Nakano et al. in view of the Related Art shown in Figure 3 by virtue of its dependence from claim 13.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: September 7, 2004

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